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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/737,124
Filing Date: December 17, 2003
Appellant(s): KIM ET AL.

John A. Castellano
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/23/2009 appealing from the Office action mailed 9/22/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,393,506	Kenny	5-2002

Definition of SDRAM from Wikipedia, undated.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

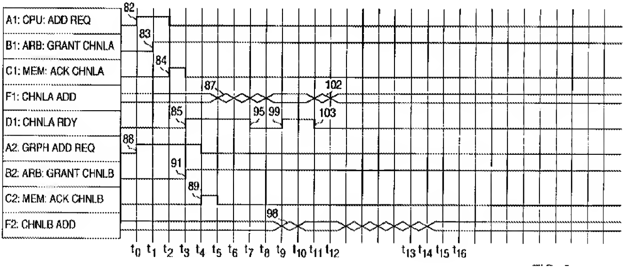
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 13-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenny.

With regard to claim 1, Kenny discloses an arbiter (arbiter 4, Fig. 1, for example) in a system (shown generally at Fig. 1) for generating a pseudo-grant signal to all requesting master units (the arbiter 4 in Kenny "assigns a virtual channel to each

master/slave pair requesting the data bus for data transfer between the master module and a slave module. Each virtual channel represents a timeslice on the bus and is owned by a separate master/slave pair, thereby permitting multiple master/slave pairs to have concurrent ownership of the singular data bus" (emphasis added). In another word, the arbiter 4 grants or bus ownership bus grant to the virtual channel of every requesting master before actual arbitration, wherein "data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate 'channel active' signal." It is clear that assigning concurrent ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual arbitration is interpreted as providing a pseudo bus grant signal by the arbiter to each master. In particular, in Kenny, a master module initializes bus access by asserting address and bus request signals on the bus 11. The arbiter 4 and the slave module detect the address and request signals asserted by the master module. The arbiter 4 then identifies the master module making the request, determines the master module's priority, and grants a virtual channel. The virtual channel granted can be arbitrarily selected by an allocation procedure. Specifically, Kenny discloses that "concurrent ownership of the data bus by multiple master/slave pairs advantageously enhances bus accessibility over conventional split-transaction bus protocols since the transactional overhead associated with bus re-acquisition protocols between a master/slave pair is eliminated. Since each channel, hence each master/slave pair, has its own unique channel active signal, data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate "channel active" signal." Kenny

further discloses that "FIG. 9 is a timing diagram summarizing concurrent transactions of three virtual channels of the present invention." In addition, Kenny discloses that "[a]ll concurrent virtual channel owners wait for an access grant by arbiter 4 to data bus 2. Access to data bus 3 to a particular virtual channel occurs when arbiter 4 asserts the virtual channel's active signal (e.g., CHNLA ACTIVE). Note that in Fig. 9, because the priority of each requesting master (CPU, PCI Controller, Graphics Controller) is not pre-assigned, the arbiter 4 must resolve the priority between requesting masters, and grants virtual channels A, B, C to each requesting master based on priority of each requesting master, by asserting signal GNT CHLNA, signal GNTCHLNB, and signal GNTCHLNC, at times t1, t3, and t5. Fig. 9 is reproduced below:

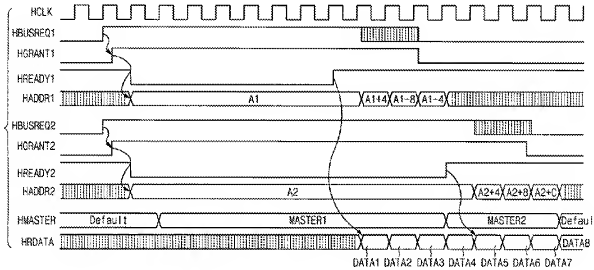


Kenny also discloses that the arbiter receives transaction information from all requesting master units in response to the pseudo-grant signals (after asserting signal

GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the requesting master).

Although Kenny clearly disclose that pseudo-grant signals are generated to all the requesting masters. Kenny, as discussed above regarding Fig. 9, does not particularly disclose that the pseudo-grant signals begin at the same time, as claimed in at least Applicants' claim 1, and shown in Fig. 6, which is reproduced below:

Fig. 6



Note that in Fig. 6 above, the pseudo-grant signals HGRANT1 and HGRANT2 begin at the same time.

However, in addition to the timing for pseudo-grant signals as shown in Fig. 9 above, Kenny also disclose that "[a]lternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and

requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere." Thus, it is clear that by using pre-designating virtual channels and priorities for each module, the arbiter 4 does not have to arbitrate between requesting masters having different priority, and assign a virtual channel to a requesting master according to its priority.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate pseudo-grant signals GNT CHLNA, GNTCHLNB, and GNTCHLNC to all requesting masters beginning at the same time, because by using a fixed virtual channel with a pre-assigned priority for each of the requesting master, the arbiter 4 does not have to arbitrate between masters resulting in generating/providing pseudo-grant signals to all requesting masters at different starting time. Since pseudo-grant signals GNT CHLNA, GNTCHLNB, and GNTCHLNC to all requesting masters begin at the same time, it is clear that arbitration latency can be further reduced, and as a result, the overall performance of the entire system of Kenny is improved.

With regard to claim 2, it is clear that the arbiter 4 further performs arbitration based on the transaction information such as the pre-assigned priority received from the requesting master.

With regard to claim 3, it is clear that in Kenny, the arbiter 4 includes a master interface for interfacing with the masters (see at least Fig. 1 and description thereof) for generating the pseudo-grant signal (virtual channel grant signal GNT CHNLA) to all the requesting masters, for receiving the transaction information from all the requesting

master units in response to the pseudo-grant signal (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the master), and for generating a ready signal (CHNLA ACTIVE, for example) to a selected one of the requesting master units. Data transaction may be performed after granting of virtual channel.

With regard to claim 4, it is clear that the master interface of arbiter 4 includes at least one generator for generating the pseudo-grant signals (GNT CHNLA) from at least one request signal (ADD/REQ) from all the requesting masters.

With regard to claim 5, it is clear that the master interface including at least one circuit for converting a target slave ready signal (CHNLA RDY) from at least one slave (also slave in Kenny) into a data transfer ready signal (CHNLA ACTIVE, for example) for a selected one of the requesting master units.

With regard to claim 6, it is clear that the ready signal (CHNLA RDY) is for data transfer.

With regard to 7, it is clear that data can only be transferred when the bus is available. In other words, the ready signal (CHNLA RDY) indeed indicates bus availability.

With regard to claim 8, it is clear that in Kenny, the arbiter including a controller interface for requesting at least one slave unit to prepare for data transfer in response to the target information (in Kenny, the target information is the address of the slave, ADD, for example) from the selected one of the requesting masters. Note that all modules as shown in Fig. 1, as in any conventional interconnected modules include

respective interface for communication among modules. See also col. 5, line 28 to col. 6, line 21).

With regard to claim 9, it is clear that the controller interface is a slave controller interface which interacts with at least one slave controller of the at least one slave unit. Note that all modules as shown in Fig. 1, as in any conventional interconnected modules) include respective interface for communication among modules. See also col. 5, line 28 to col. 6, line 21).

With regard to claim 10, it is clear that slave memory 6 includes slave controller to control the slave memory.

With regard to claim 13, each driver layer 12 of each master includes registers 21, 22 and 23. Registers 21, 22, and 23 latch read, address and write data, respectively. A master or system clock FCLK (not shown), is received at terminal 24 to synchronize registers 21, 22 and 23 with timing on the bus.

With regard to claims 14-39, see discussion above, since the subject matter presented in claims 14-39 has already been addressed. With regard to claim 29, note also that it is clear from the discussion above that the steps of generating the request from the master, receiving the request and generating a virtual channel grant signal from the arbiter 4, supplying information from the master, and preparing for data transfer constitute a first stage and completing and transferring constitute a second stage and the first and second stage occur concurrently.

With regard to claim 40, not only pre-assigned priority, but also priority scheme such as dynamic priority is disclosed.

With regard to claim 41, in Kenny, it is clear that information from the target slave is also used. It is clear that the master interface including at least one circuit for converting a target slave ready signal (CHNLA RDY) from at least one slave (also slave in Kenny) into a data transfer ready signal (CHNLA ACTIVE, for example) for a selected one of the requesting master units. See at least column 5, lines 57-63; column 6, line 62 to column 8, line 60.

With regard to claims 42 and 43, see discussion regarding claim 3 above.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenny as discussed above, and further in view of the following.

Kenny, as discussed above, discloses the claimed invention including the use of interface controllers for the arbiter and slave module such as the memory module 6. Kenny does not disclose the use of SDRAM (Synchronous Dynamic Random Access Memory). However, memory such as SRAM is old and well-known in the art as evidence by the definition of SDRAM provided by Wikipedia.com, cited previously. SDRAM is an improvement to standard DRAM in that it retrieves data alternately between two sets of memory. This eliminates the delay caused when one bank of addresses is shut down while another is prepared for reading. It's called "Synchronous" DRAM because the memory is synchronized with the clock speed that the computer's CPU bus speed is optimized for. The faster the bus speed, the faster the SDRAM can be. In other words, SDRAM's timing is synchronized to the system clock. By running in sync to an external clock signal, SDRAM can run at the same speed as the

CPU/memory bus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ SRAM in memory module 6 of Kenny, since the use of SDRAM is old and well-known, as evidence by the definition of SDRAM provided by Wikipedia.com, cited previously, for improving latency. Note also that since the interface controller of the arbiter 4 is in direct communication with the memory slave 6 SDRAM controller, it is clear that controller interface is an SDRAM controller interface which interacts with at least one SDRAM controller of the at least one slave unit.

(10) Response to Argument

Part A:

In part A, Appellants provide a general discussion of Kenney, <u>as understood by Appellants,</u> without specifically address any supposed error in the Final Rejection. Therefor, no further response is deemed necessary.

Part B:

<u>Appellants' argument 1:</u>

<u>1. KENNY FAILS TO DISCLOSE OR FAIRLY SUGGEST "AT LEAST ONE INTERFACE FOR GENERATING PSEUDO-GRANT SIGNALS TO ALL REQUESTING MASTER UNITS BEGINNING AT THE SAME TIME AND FOR RECEIVING TRANSACTION INFORMATION FROM ALL REQUESTING MASTER UNITS IN RESPONSE TO THE PSEUDO-GRANT SIGNALS" AS REQUIRED BY CLAIM 1.</u>

Appellants have argued that "in Kenny the master module 5 initializes bus access by asserting an address and bus request signal (ADD/REQ) on the bus 11. Only after receiving the address and bus request signal (ADD/REQ) does the arbiter 4 assert the

virtual channel grant signal to the requesting master module 5. To meet the limitations of claim 1, the arbiter 4 of Kenny must '[generate] pseudo-grant signals [and receive] transaction information from all requesting master units/n response to the pseudo-grant signals.' But, as described above this is not the case. Only after receiving the address and bus request signal (ADD/REQ) does the arbiter 4 assert the virtual channel grant signal to the requesting master module 5. Kenny does not disclose (either explicitly or implicitly), that the arbiter 4 asserts any signal, let alone a pseudo grant signal, prior to receiving the address and bus request signal (ADD/REQ) from the master module 5. Indeed, Kenny utilizes the term 'initializes' to refer to the assertion of the address and bus request signal (ADD/REQ) from the master module 5, which indicates this to be the first or initial step in the process. The logical conclusion from the use of the term 'initialize' is that the master module 5 asserts the address and bus request signals prior to receiving any signals from the arbiter 4, let alone, a 'pseudo-grant signal.' This conclusion is further supported by FIG. 6 of Kenny. As shown in FIG. 6, the arbiter 4 transitions from an initial state 47 to state 48 (in which a virtual channel grant is asserted) only after receiving the address and bus request signal (including the address of the slave) from the master module. Kenny at 7:34-40. In other words, FIG. 6 also shows that the address and bus request signal is issued by the master module prior to (not after or in response to) the virtual channel grant from the arbiter 4. Indeed, it is the virtual channel grant that is asserted by the arbiter 4 in response to the address and bus request signal from the master module, not vice versa. Further still, FIG. 9A of Kenny also supports that the virtual channel grant is issued only after receiving an address and

bus request signal (ADD/REQ) signal from the master module… As Kenny states in describing FIG. 9A, the 'arbiter 4 ... grants virtual channels A, B and C ... by asserting signal GNT CHLNA, signal GNT CHLNB, and GNT CHLNC.' Kenny at 9:53-56. Clearly, one can appreciate from FIG. 9A that the granting of the virtual channels A, B, and C occurs after receiving respective address and bus request signals (CPU: ADD REQ and GRPH: ADD REQ) from the requesting master modules CPU and GRPH. In sum, from review of FIGS. 5, 6 and 9A, one can appreciate that the arbiter 4 of Kenny does not receive the address and bus request signal from the master module in response to the virtual channel grant from the arbiter 4. Rather, in Kenny the arbiter 4 receives the address and bus request signal prior to asserting the virtual channel grant … Referring again to FIG. 6 of Kenny, upon detecting the address and bus request signal from the master module, the arbiter 4 asserts grant channel A signal GNT CHNLA on address bus 3 to assign a virtual channel to master module. Kenny at 7:34-7:37. After transmitting the virtual grant channel signal GNT CHNLA, the arbiter 4 returns to its initial state 47 to wait for the next address and bus request signal. Id. at 41-42. But, the next address and bus request signal received by the arbiter 4 is from a different master module (see, Kenny at FIG. 9A), and therefore, is independent of- not in response to - the grant channel A signal GNT CHNLA from the arbiter 4. Thus, contrary to the Examiner's assertion, the arbiter 4 does not receive the address and bus request signal from a master module 4 in response to the virtual channel grant as required to meet the limitations of claim 1… Kenny does not disclose that the subsequent address and bus request signal (ADD/REQ) is in any way related to (and thus is not in response to) the

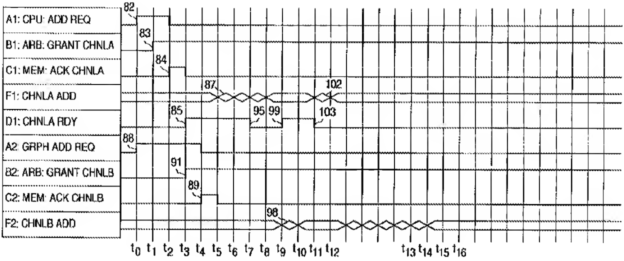
prior virtual channel grant signal from the arbiter 4. In sum, at most FIGS. 5 and 6 of Kenny disclose that the master modules assert address and bus request signals to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT CHNLC in Kenny are provided only after receiving address and bus request signals from respective requesting master modules ... Assuming arguendo that assignment of a virtual channel in Kenny was similar to the 'pseudo grant signal' of claim 1, the arbiter 4 of Kenny still does not receive 'transaction information from all requesting master units in response to the pseudo-grant signals' as required to meet the limitations of claim 1. As discussed above, the master modules in Kenny are not aware of the virtual channels that have been assigned by the arbiter 4 until the arbiter 4 issues a GNT CHNLA (Kenny at 9:53-56), which is provided only after receiving the address and bus request signal from a requesting master module. Therefore, the arbiter of Kenny does not receive transaction information in response to pseudo-grant signals as required to meet the limitations of claim 1."

In response to Appellants' argument, at the outset, it is important to note that a <u>"pseudo-grant signal" is not an actual grant signal from an arbiter. The "pseudo-grant signal" is a pre-grant signal provided to each of the requesting master units</u>. It is also important to note that in Kenny, assigning <u>concurrent</u> ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual arbitration **<u>is interpreted as providing a pseudo bus grant signal by the arbiter to each master</u>**.

The only difference between the claimed subject matter of that of Kenny is that Kenny does not explicitly disclose that the pseudo-grant signal is provided to each requesting master unit at the same time." Further, in Kenny, actual arbitration performed by arbiter 4 requires the information from all requesting masters. The “transaction information” (claim 1) from each master includes address of the target and/or priority of the target (ADD/REQ). See at least column 5, lines 57-63; column 6, line 58 to column 7, line 65.

Contrary to Appellants’ argument, the arbiter 4 in Kenny "assigns a virtual channel to each master/slave pair requesting the data bus for data transfer between the master module and a slave module. Each virtual channel represents a timeslice on the bus and is owned by a separate master/slave pair, thereby permitting multiple master/slave pairs to have concurrent ownership of the singular data bus" (emphasis added). In other words, the arbiter 4 grants or bus ownership bus grant to the virtual channel of every requesting master before actual arbitration, wherein "data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate 'channel active' signal." It is clear that assigning concurrent ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual arbitration **is interpreted as providing a pseudo bus grant signal by the arbiter to each master**. In particular, in Kenny, a master module initializes bus access by asserting address and bus request signals on the bus 11. The arbiter 4 and the slave module detect the address and request signals asserted by the master module. The arbiter 4 then identifies the master module making the request, determines the master module's priority, and grants a virtual channel. The virtual channel granted can be

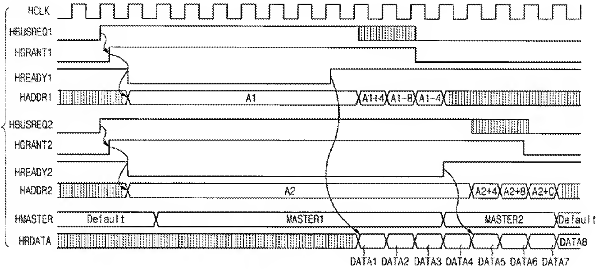
arbitrarily selected by an allocation procedure. Specifically, Kenny discloses that "concurrent ownership of the data bus by multiple master/slave pairs advantageously enhances bus accessibility over conventional split-transaction bus protocols since the transactional overhead associated with bus re-acquisition protocols between a master/slave pair is eliminated. Since each channel, hence each master/slave pair, has its own unique channel active signal, data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate "channel active" signal." Kenny further discloses that "FIG. 9 is a timing diagram summarizing concurrent transactions of three virtual channels of the present invention." In addition, Kenny discloses that "[a]ll concurrent virtual channel owners wait for an access grant by arbiter 4 to data bus 2. Access to data bus 3 to a particular virtual channel occurs when arbiter 4 asserts the virtual channel's active signal (e.g., CHNLA ACTIVE). Note that in Fig. 9, because the priority of each requesting master (CPU, PCI Controller, Graphics Controller) is not pre- assigned, the arbiter 4 must resolve the priority between requesting masters, and grants virtual channels A, B, C to each requesting master based on priority of each requesting master, by asserting signal GNT CHLNA, signal GNTCHLNB, and signal GNTCHLNC, at times t1, t3, and t5. Fig. 9 is reproduced below:



Kenny also discloses that the arbiter receives transaction information from all requesting master units in response to the pseudo-grant signals (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the requesting master). Further discussion is provided below.

Although Kenny clearly discloses that pseudo-grant signals are generated to all the requesting masters. Kenny, as discussed above regarding Fig. 9, does not particularly disclose that the pseudo-grant signals begin at the same time, as claimed in at least Applicants' claim 1, and shown in Appellants' Fig. 6, which is reproduced below:

Fig. 6



Note that in Appellants' Fig. 6 above, the pseudo-grant signals HGRANT1 and HGRANT2 begin at the same time.

However, in addition to the timing for pseudo-grant signals as shown in Fig. 9 above, Kenny also disclose that "[a]lternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere." Thus, it is clear that by using pre-designating virtual channels and priorities for each module, the arbiter 4 does not have to determine assignment of the virtual channels to the modules (masters). As a result the arbiter 4 can send pseudo grant signals GNT CHNL to the requesting masters A, B,

C at the same time. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate pseudo-grant signals GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting masters beginning at the same time, because by using a fixed virtual channel with a pre-assigned priority for each of the requesting master, the arbiter 4 does not have to arbitrate between masters resulting in generating/providing pseudo-grant signals to all requesting masters at different starting time. Since pseudo-grant signals GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting masters begin at the same time, it is clear that arbitration latency can be further reduced, and as a result, the overall performance of the entire system of Kenny is improved.

Further, in Kenny, actual arbitration performed by arbiter 4 requires the information from all requesting masters. The information from the master includes address of the target and/or priority of the target (ADD/REQ). See at least column 5, lines 57-63; column 6, line 58 to column 7, line 65. Thus, contrary to Appellants' argument, it is clear from Kenny, particularly from Kenny's Fig. 6, which is reproduced below for ease of reference and convenience, that the next ADD/REQ is not independent. As a matter of fact, the next ADD/REQ would not be sent to the arbiter without reception of the pseudo grant GNT CHNL signal. In other words, ADD/REQs (transaction information) from requesting masters are sent to the arbiter in response to the pseudo-grant signals GNT CHNL.

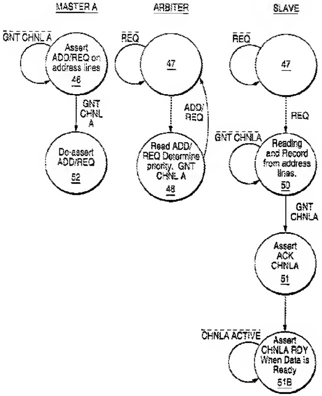


Fig. 6

As clearly shown in Fig. 6 above, upon receiving the GNT CHNL A signal, the <u>ADD/REQ is de-asserted</u>. At a subsequent arbitration cycle, since the ADD/REQ is de-asserted by the GNT CHNL A signal, the ADD/REQ must be asserted.

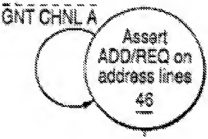
The process can be illustrated in the following diagram:

GNT CHNL A -----------> DE-ASSERT ADD/REQ ------------> ASSERT ADD/REQ

Thus, it is clear that the ADD/REQ ("transaction information") is received in response to the pseudo-grant signal (GNT CHNL A).

As a mater of fact, as clearly shown in Fig. 6 (a portion of which is reproduced below for clarity), the ADD/REQ ("transaction information") is received in response to the pseudo grant signal GNT CHNL A.

MASTER A



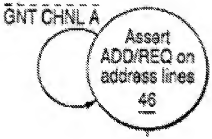
It is also important to note that the Kenny Rejection is a rejection under section 103, wherein the "pseudo grant signals" (GNT CHNL or Grant Channel Signals) are sent to masters A, B, and C <u>at the same time</u>. Thus, the respective ADD/REQs of the respective masters A, B, and C are de-asserted at the same time upon receiving concurrent "pseudo grant signals" (GNT CHNL or Grant Channel Signals) sent to masters A, B. and C. At a subsequent arbitration cycle, since the ADD/REQs are de-asserted by the concurrent pseudo signals GNT CHNL, the ADD/REQs must be asserted.

The process can be illustrated in the following diagram:

GNT CHNL (A, B, C) -----------> DE-ASSERT ADD/REQ (A, B, C) ------------> ASSERT ADD/REQ (A, B, C)

Take master A (Fig. 6 of Kenny above for example), the ADD/REQ ("transaction information") is received in response to the pseudo grant signal GNT CHNL A.

<u>MASTER A</u>



In other words, the pseudo-grant signals GNT CHNL (A, B, C) are generated to all requesting master units (A, B, C) beginning at the same time and for receiving transaction information (ADD/REQ (A, B, C)) from all requesting master units (A, B. C) in response to the pseudo-grant signals GNT CHNL (A, B, C).

<u>Appellants' argument 2:</u>

<u>2. "[GENERATING] PSEUDO-GRANT SIGNALS TO ALL REQUESTING MASTER UNITS BEGINNING AT THE SAME TIME" AS REQUIRED BY CLAIM 1 IS NOT OBVIOUS IN VIEW OF KENNY.</u>

Appellants have argued that "the Examiner fails to recognizes that modifying Kenny as suggested would change the principle of operation of Kenny because the

system of Kenny issues virtual grant signals sequentially according to priority of the requesting master modules. If Kenny were to be modified as suggested by the Examiner, the virtual channels would no longer be granted according to a master module's priority, thereby significantly changing the principle operation of the system of Kenny; namely prioritizing bus ownership. Because the Examiner's suggested modification would change the principle operation of Kenny, the teachings of Kenny are not sufficient to render claim 1 prima facie obvious."

In response to Appellants' argument, at the outset, it is noted that there is no evidence suggesting that "teachings of Kenny are not sufficient to render claim 1 prima facie obvious." To the contrary, <u>ample evidence set forth above proves that the teachings of Kenny are clearly sufficient to render claim 1 obvious.</u>

Specifically, contrary to Appellants' argument, in addition to the timing for pseudo-grant signals as shown in Fig. 9 above, Kenny also disclose that "[a]lternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere." Thus, it is clear that by using <u>pre-designating virtual channels and priorities</u> for each module, the arbiter 4 <u>does not</u> have to determine assignment of the virtual channels to the modules (masters). As a result the arbiter 4 can send pseudo grant signals GNT CHNL to the requesting masters A, B, C at the same time. Thus, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to generate pseudo-grant signals GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting masters beginning at the same time, because by using a fixed virtual channel with a pre-assigned priority for each of the requesting master, the arbiter 4 does not have to arbitrate between masters resulting in generating/providing pseudo-grant signals to all requesting masters at different starting time. Since pseudo-grant signals GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting masters begin at the same time, it is clear that arbitration latency can be further reduced, and as a result, the overall performance of the entire system of Kenny is improved.

Appellants' argument 3:

3. FURTHER ARGUMENTS AGAINST THE EXAMINER'S REJECTION.

Appellants have further argued that "if the arbiter 4 of Kenny need not arbitrate between requesting masters (as suggested by the Examiner), then the arbiter 4 of Kenny does not 'perform arbitration based on the information on the target slave unit for each requesting master unit by using the information on the target slave unit for each requesting master unit to determine a priority of bus ownership for the requesting master units' after generating pseudo- grant signals and receiving transaction information in response to the pseudo-grant signals as is required to meet the limitations of claim 1. Further still, even assuming arguendo that the arbitration performed by the arbiter 4 of Kenny depends from the address of the target and/or priority of the target from the requesting master module as suggested by the Examiner

(which Appellants do not admit), the address and/or priority of the target slave still does not constitute the 'transaction information,' of claim 1 because this information is received prior to the grant of the virtual channel, but not 'in response to,' the grant of the virtual channel. Kenny at 6:63 - 7:4. For at least these additional reasons, Kenny fails to render claim 1 obvious."

In response to Appellants' argument, <u>in Kenny, it is important to distinguish between assigning virtual channels (pseudo grant) to masters by the arbiter 4 and actual arbitration between the masters performed by the arbiter 4, which requires the "transaction information" such as the address of the target and/or priority of the target.</u>

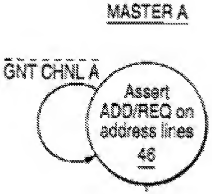
Further, contrary to Appellants' argument, as discussed above in conjunction with Fig. 6 of Kenny, upon receiving the GNT CHNL A signal, the <u>ADD/REQ is de-asserted</u>. At a subsequent arbitration cycle, since the ADD/REQ is de-asserted by the GNT CHNL A signal, the ADD/REQ must be asserted.

The process can be illustrated in the following diagram:

GNT CHNL A ----------> DE-ASSERT ADD/REQ -----------> ASSERT ADD/REQ

Thus, it is clear that the ADD/REQ ("transaction information") is received in response to the pseudo-grant signal (GNT CHNL A).

As a mater of fact, as clearly shown in Fig. 6 (a portion of which is reproduced below for clarity), the ADD/REQ ("transaction information") is received in response to the pseudo grant signal GNT CHNL A.



Thus, it is clear that in Kenny, the transaction information is received in response to the grant of the virtual channel (pseudo grant).

Appellants' argument 4:

4. CONCLUSION WITH RESPECT TO CLAIM 1.

Since Appellants do not address any supposed error in the Final Rejection, no further response is deemed necessary.

"Part B": (incorrectly labeled by Appellants, part B should have been Part C)

Appellants have argued that Claims 2-13, 40, 41, and 42 depend from independent claim 1. Therefore, these claims are not anticipated or rendered obvious at least by virtue of their dependency.

In response to Appellants' argument, since Appellants do not separately argue against claims 2-13, 40, 41, and 42, no further response is dimmed necessary.

<u>"Part C":</u> (incorrectly labeled by Appellants, part C should have been Part D)

With regard to claims 14-18 and 37, Appellants have argued that "[a]s discussed above, at most FIGS. 5 and 6 of Kenny disclose that a master module asserts the address and bus request signal (ADD/REQ) to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT CHNLC in Kenny are provided only after receiving respective address and bus request signals from respective requesting master modules. By contrast, in claim 14 the arbiter generates "pseudo-grant signals to all requesting master units" and the at least two master units supply "transaction information from all requesting master units /n response to the pseudo-grant signals." The arbiter 4 of Kenny surely cannot be said to receive transaction information in response to a pseudo-grant signal if the arbiter 4 does not assert any virtual channel grant signal prior to receiving the address and bus request signal from the master module. Further, as discussed above with regard to claim 1, modifying Kenny such that the virtual channel grant signals are generated at the same time would change the principle operation of the system of Kenny; namely prioritizing bus ownership."

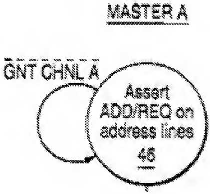
Contrary to Appellants' argument, as discussed above regarding claim 1, as shown in Fig. 6 of Kenny, upon receiving the GNT CHNL A signal, the <u>ADD/REQ is de-asserted</u>. At a subsequent arbitration cycle, since the ADD/REQ is de-asserted by the GNT CHNL A signal, the ADD/REQ must be asserted.

The process can be illustrated in the following diagram:

GNT CHNL A ----------> DE-ASSERT ADD/REQ -----------> ASSERT ADD/REQ

Thus, it is clear that the ADD/REQ ("transaction information") is received in response to the pseudo-grant signal (GNT CHNL A).

As a mater of fact, as clearly shown in Fig. 6 (a portion of which is reproduced below for clarity), the ADD/REQ ("transaction information") is received in response to the pseudo grant signal GNT CHNL A.



Thus, it is clear that in Kenny, the transaction information is received in response to the grant of the virtual channel (pseudo grant).

In addition, in response to Appellants' argument that "modifying Kenny such that the virtual channel grant signals are generated at the same time would change the principle operation of the system of Kenny," it is clear from discussion above that in addition to the timing for pseudo-grant signals as shown in Fig. 9 above, Kenny also disclose that "[a]lternatively, each subsystem may be configured with a fixed virtual

channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere." Thus, it is clear that by using pre-designating virtual channels and priorities for each module, the arbiter 4 does not have to determine assignment of the virtual channels to the modules (masters). As a result the arbiter 4 can send pseudo grant signals GNT CHNL to the requesting masters A, B, C at the same time. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate pseudo-grant signals GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting masters beginning at the same time, because by using a fixed virtual channel with a pre-assigned priority for each of the requesting master, the arbiter 4 does not have to arbitrate between masters resulting in generating/providing pseudo-grant signals to all requesting masters at different starting time. Since pseudo-grant signals GNT CHLNA, GNT CHLN B, and GNT CHLN C to all requesting masters begin at the same time, it is clear that arbitration latency can be further reduced, and as a result, the overall performance of the entire system of Kenny is improved.

"Part D:" (incorrectly labeled by Appellants, part D should have been Part E)

Appellants' arguments regarding claims 19-25, 34, and 35 are identical to Appellants' argument regarding claims 14-18, and 37 above. Thus, in response to

Appellants' argument, see the Examiner's response regarding claims 14-18, and 37 above.

"Part E:" (incorrectly labeled by Appellants, part E should have been Part F)

Appellants' arguments regarding claims 26-33, 35, and 39 are identical to Appellants' argument regarding claims 14-18, and 37 above. Thus, in response to Appellants' argument, see the Examiner's response regarding claims 14-18, and 37 above.

"Part F:" (incorrectly labeled by Appellants, part F should have been Part G)

Appellants' arguments regarding claim 43 are identical to Appellants' argument regarding claims 14-18, and 37 above. Thus, in response to Appellants' argument, see the Examiner's response regarding claims 14-18, and 37 above.

"Part G:" (incorrectly labeled by Appellants, part G should have been Part H)

With regard to claims 11 and 12, Appellants have argued that "[t]he Examiner rejects claims 11-12 as unpatentable over Kenny in view of the Examiner's citation of Wikipedia and the comments set forth on pages 9 and 10 of the Final Rejection. Appellants continue to challenge the Examiner's citation of Wikipedia as sufficient teaching to establish that a particular teaching was well-known in the art at the time of the invention. Wikipedia is an open content encyclopedia the contents of which can be edited by anyone. Moreover, Appellants also challenge the Examiner's mere comments

or Official Notice on page 9 of the Final Rejection that the features of claims 11 and 12 would have been obvious. Regardless, however, claims 11 and 12 are patentable by virtue of their dependency from claim 1."

Contrary to Appellants' argument, SDRAM "began its path to universal acceptance" in 1993 (see definition of SDRAM by Wikipedia, under "SDRAM history"). Thus, it is clear that SDRAM is well-known in the art at the time of Appellants' alleged invention. Further, while the Examiner agrees with Appellants that "Wikipedia is an open content encyclopedia," it is common knowledge that information provided by Wikipedia is verified by citations and references provided at the end of each Wiki document. As clearly discussed above and in the rejection of claim 11 and 12, memory such as SDRAM is old and well-known in the art since 1993. SDRAM is an improvement to standard DRAM in that it retrieves data alternately between two sets of memory. This eliminates the delay caused when one bank of addresses is shut down while another is prepared for reading. It's called "Synchronous" DRAM because the memory is synchronized with the clock speed that the computer's CPU bus speed is optimized for. The faster the bus speed, the faster the SDRAM can be. In other words, SDRAM's timing is synchronized to the system clock. By running in sync to an external clock signal, SDRAM can run at the same speed as the CPU/memory bus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ SRAM in memory module 6 of Kenny, since the use of SDRAM for improving latency is old and well-known since 1993. Note also that in Kenny, the arbiter 4 comprises a slave interface directly interfacing and controlling/communicating with

SDRAM memory 6 via SDRAM interface layers. Thus, it is clear that the slave controller interface in Kenny can be called “SDRAM controller interface.”

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner’s answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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